8. (Amended) The high speed DRAM of claim 7, wherein an eleventh data bus couples the DRAM memory to a write buffer which is coupled through the third data bus to the write register.

13. (Amended) A method of operating the high speed DRAM of claim 3, wherein for a read miss operation, a new set of data are retrieved from the DRAM memory to replace old data in the cache memory, and also to be sent to outside data buses through an output read buffer, and during a first cycle of data flow, data flows from the cache memory through the first and fourth buses and is latched into the read register, and data coming from the DRAM memory are latched into the write register through the third bus, and in a second cycle, the directional flows of the data are reversed through the first and fourth buses and also through the third bus.

REMARKS

Claims 4, 8 and 13 have been amended to obviate the rejections thereof under 35 USC 112.

Reconsideration is respectfully requested of the rejection of claims 1-2 and 4-21 under 35 USC 102(e) as being anticipated by Leung (USPN: 6,415,353), and the rejection of claim 3 under 35 USC 103(a) as being unpatentable over Leung, particularly for the following reasons.

Leung Compared To The Invention

The design objective of Leung is basically to hide a data refresh cycle, whereas the design objective of the present invention is to minimize the cycle time to access data over